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☐ 1. **Test development for a third-version ColdFire microprocessor**
Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;
Design & Test of Computers, IEEE
Volume 17, Issue 4, Oct.-Dec. 2000 Page(s):29 - 37

AbstractPlus | References | Full Text: PDF(152 KB)   IEEE JNL

☐ 2. **The testability features of the 3rd generation ColdFire(R) family of microprocesso**
Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;
Test Conference, 1999. Proceedings. International
28-30 Sept. 1999 Page(s):913 - 922

AbstractPlus | Full Text: PDF(800 KB)   IEEE CNF

☐ 3. **On-the-shelf core pattern methodology for ColdFire(R) microprocessor cores**
McLaurin, T.L.; Potter, J.C.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):1100 - 1107

AbstractPlus | Full Text: PDF(668 KB)   IEEE CNF

☐ 4. **The testability features of the MCF5407 containing the 4th generation ColdFire(R microprocessor core**
McLaurin, T.L.; Frederick, F.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):151 - 159

AbstractPlus | Full Text: PDF(552 KB)   IEEE CNF

☐ 5. **The testability features of the ARM1026EJ microprocessor core**
McLaurin, T.L.; Frederick, F.; Slobodnik, R.;
Test Conference, 2003. Proceedings. ITC 2003. International
Volume 1, Sept. 30-Oct. 2, 2003 Page(s):773 - 782

AbstractPlus | Full Text: PDF(919 KB)   IEEE CNF

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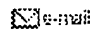**Welcome United States Patent and Trademark Office**

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☐ 1. **ETM10 incorporates hardware segment of IEEE P1500**
McLaurin, T.; Ghosh, S.;
Design & Test of Computers, IEEE
Volume 19, Issue 3, May-June 2002 Page(s):6 - 11

AbstractPlus | References | Full Text: PDF(245 KB) **IEEE JNL**

☐ 2. **Test development for a third-version ColdFire microprocessor**
Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;
Design & Test of Computers, IEEE
Volume 17, Issue 4, Oct.-Dec. 2000 Page(s):29 - 37

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Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;
Test Conference, 1999. Proceedings. International
28-30 Sept. 1999 Page(s):913 - 922

AbstractPlus | Full Text: PDF(800 KB) **IEEE CNF**

☐ 4. **Preliminary Outline of the IEEE PI 500 Scalable Architecture for Testing Embedde**
Adham, S.; Burek, D.; Clark, C.J.; Collins, M.; Giles, G.; Sales, A.; Marinissen, E.J.; Mc
Monzel, J.; Muradali, F.; Rajoki, J.; Rajsuman, R.; Ricchatti, M.; Stannard, D.; Udell, J.;
Whetsel, L.; Zamfirescu, A.; Zorian, Y.;
VLSI Test Symposium, 1999. Proceedings. 17th IEEE
25-29 April 1999 Page(s):483 - 488

AbstractPlus | Full Text: PDF(436 KB) **IEEE CNF**

☐ 5. **On-the-shelf core pattern methodology for ColdFire(R) microprocessor cores**
McLaurin, T.L.; Potter, J.C.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):1100 - 1107

AbstractPlus | Full Text: PDF(668 KB) **IEEE CNF**

☐ 6. **The testability features of the MCF5407 containing the 4th generation ColdFire(R**
microprocessor core
McLaurin, T.L.; Frederick, F.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):151 - 159

AbstractPlus | Full Text: PDF(552 KB)   IEEE CNF

☐   7.   **The testability features of the ARM1026EJ microprocessor core**
McLaurin, T.L.; Frederick, F.; Slobodnik, R.;
Test Conference, 2003. Proceedings. ITC 2003. International
Volume 1, Sept. 30-Oct. 2, 2003 Page(s):773 - 782

AbstractPlus | Full Text: PDF(919 KB)   IEEE CNF

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Original Classifications
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11   714/726
 5   714/718
 3   714/727
 2   365/201
 2   708/130
 2   714/733
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Cross-Reference Classifications
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 5   714/733
 5   714/734
 4   324/73.1
 4   714/724
 4   714/726
 3   365/201
 3   714/727
 2   324/763
 2   712/37
 2   714/731
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Combined Classifications
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15   714/726
 7   714/733
 6   714/718
 6   714/727
 5   365/201
 5   714/724
 5   714/734
 4   324/73.1
 3   712/37
 2   324/763
 2   365/233
 2   365/49
 2   708/130
 2   714/731
 2   714/736
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Titles of Most Frequently Occurring Classifications of Patents Returned
From A Search of 10812309 on June 17, 2005

15 714/726   (11 OR, 4 XR)
            Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
            714/699   PULSE OR DATA ERROR HANDLING
            714/724   .Digital logic testing
            714/726   ..Scan path testing (e.g., level sensitive scan
                              design (LSSD))

 7 714/733   (2 OR, 5 XR)
            Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
            714/699   PULSE OR DATA ERROR HANDLING
            714/724   .Digital logic testing
            714/733   ..Built-in testing circuit (BILBO)

 6 714/718   (5 OR, 1 XR)
            Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
            714/699   PULSE OR DATA ERROR HANDLING
            714/718   .Memory testing

 6 714/727   (3 OR, 3 XR)
            Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
            714/699   PULSE OR DATA ERROR HANDLING
            714/724   .Digital logic testing
            714/726   ..Scan path testing (e.g., level sensitive scan
                              design (LSSD))
            714/727   ...Boundary scan

 5 365/201   (2 OR, 3 XR)
            Class   365 : STATIC INFORMATION STORAGE AND RETRIEVAL
            365/189.01   READ/WRITE CIRCUIT
            365/201   .Testing

 5 714/724   (1 OR, 4 XR)
            Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
            714/699   PULSE OR DATA ERROR HANDLING
            714/724   .Digital logic testing

 5 714/734   (0 OR, 5 XR)
            Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
            714/699   PULSE OR DATA ERROR HANDLING
            714/724   .Digital logic testing
            714/734   ..Structural (in-circuit test)

 4 324/73.1   (0 OR, 4 XR)
            Class   324 : ELECTRICITY: MEASURING AND TESTING
            324/73.1   PLURAL, AUTOMATICALLY SEQUENTIAL TESTS

 3 712/37   (1 OR, 2 XR)
            Class   712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                            SYSTEMS: PROCESSING ARCHITECTURES AND   INSTRUCTION
                            PROCESSING
            712/1   PROCESSING ARCHITECTURE
            712/32   .Microprocessor or multichip or multimodule
                              processor having sequential program control

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        712/37          ..Programmable (e.g., EPROM)

2  324/763          (0 OR, 2 XR)
        Class   324 :  ELECTRICITY:  MEASURING AND TESTING
        324/500         FAULT DETECTING IN ELECTRIC CIRCUITS AND OF
                            ELECTRIC COMPONENTS
        324/537         .Of individual circuit component or element
        324/763         ..DUT including test circuit

2  365/233          (1 OR, 1 XR)
        Class   365 :  STATIC INFORMATION STORAGE AND RETRIEVAL
        365/230.01      ADDRESSING
        365/233         .Sync/clocking

2  365/49           (1 OR, 1 XR)
        Class   365 :  STATIC INFORMATION STORAGE AND RETRIEVAL
        365/49          ASSOCIATIVE MEMORIES

2  708/130          (2 OR, 0 XR)
        Class   708 :  ELECTRICAL COMPUTERS:  ARITHMETIC PROCESSING
                            AND CALCULATING
        708/100         ELECTRICAL DIGITAL CALCULATING COMPUTER
        708/130         .Programmable calculator

2  714/731          (0 OR, 2 XR)
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                            DETECTION/RECOVERY
        714/699         PULSE OR DATA ERROR HANDLING
        714/724         .Digital logic testing
        714/726         ..Scan path testing (e.g., level sensitive scan
                            design (LSSD))
        714/731         ...Clock or synchronization

2  714/736          (1 OR, 1 XR)
        Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
        714/699         PULSE OR DATA ERROR HANDLING
        714/724         .Digital logic testing
        714/736         ..Device response compared to expected
                            fault-free response
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PLUS Search Results for S/N 10812309, Searched June 17, 2005

The Patent Linguistics Utility System (PLUS) is a USPTO automated search
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query-by-example search system which produces a list of patents that are
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L2	4183	324/537,763,765.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/17 12:14
L3	4308	714/724,726,727,729,733,734, 718.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/17 12:15
L4	8620	1 or 2 or 3	US-PGPUB; USPAT	OR	ON	2005/06/17 12:15

Method
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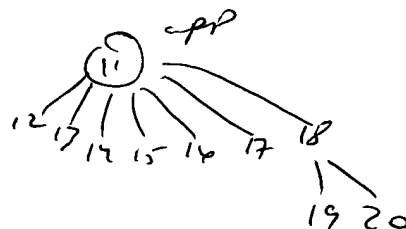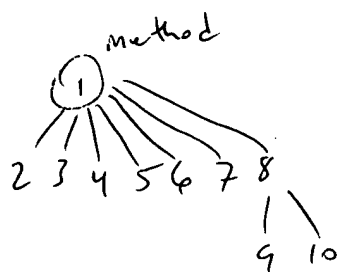
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